MULTIMEDIA UNIVERSITY

STUDENT ID NO

MULTIMEDIA UNIVERSITY

FINAL EXAMINATION

TRIMESTER 2, 2018/2019

EEN1036 –DIGITAL LOGIC DESIGN

(TE/RE)

12 MARCH 2019
02:30 p.m – 04:30 p.m
(2 Hours)

INSTRUCTION TO STUDENTS

1. This Question paper consists of 6 pages (including cover page) with **4** Questions only.

2. Attempt **ALL FOUR** questions. All questions carry equal marks and the distribution of the marks for each question is given.

3. Please write all your answers in the Answer Booklet provided.

Question 1

(a) In a digital system, data can be transmitted either via parallel or serial transmission. Discuss the meaning of parallel and serial transmission respectively.

[2 marks]

(b) Complete the following table by converting the numbers from the given base to the other three bases listed in the table

Decimal	Binary	Octal	Hexadecimal
187.25			
		130.4	
			B.C

[9 marks]

(c) Convert the two numbers 221_8 and 13_8 to binary representation. Subsequently, perform the operation of $221_8 \div 13_8$ in binary.

[6 marks]

(d) Encode the decimal number of 83_{10} in

(i) Binary Coded Decimal (BCD)

[2 marks]

(ii) Excess-3 Code

[3 marks]

(iii) Gray Code

[3 marks]

Continued...

Question 2

(a) Prove the following expressions:

(i) $Q = \overline{A}.B + \overline{A}.B.C + \overline{A}.B.D + C.D + D = \overline{A}.B + D$

[4 marks]

(ii) $Q = \overline{\left((A + \overline{B}).C\right)}\left(A + B\right)\overline{\left(C + A\right)} = \overline{A}B\overline{C}$

[6 marks]

(b) Use Karnaugh map techniques to simplify

$Y = \overline{A}.\overline{B}.\overline{C}.D + \overline{A}.B.\overline{C}.D + A.B.\overline{C}.D + A.\overline{B}.\overline{C}.D + A.B.C.D$

[5 marks]

(c) Given that the Boolean expression, $Z = \left(A.\overline{B} + B\right)B + A$.

(i) Draw the logic circuit diagram for the Boolean expression.

[4 marks]

(ii) Construct the truth table of Z.

[4 marks]

(iii) Simplify and prove that $Z = A + B$.

[2 marks]

Continued...

Question 3

(a) A particular sequential circuit with the state table as shown in Table Q3A is given.

Table Q3A

Present State M_tN_t	Input I	Next State $M_{t+1}N_{t+1}$	Output O
00	0	01	0
00	1	11	0
01	1	11	0
01	0	10	1
10	0	01	1
10	1	00	0
11	1	00	0
11	0	10	0

(i) Draw the state diagram of the sequential circuit based on the state table as shown in Table Q3A. Clearly label the states and each transition together with the inputs and outputs.

[8 marks]

(ii) By using two D flip-flops and standard combinational logic gates, implement the state table as in Table Q3A where the first flip-flop is used to generate the next state M_{t+1} while the second flip-flop is used to generate the next state N_{t+1}. By using K-map simplification approach, find the sum-of-product expressions for the D input to each of the D flip-flop without drawing the circuit implementation.

[8 marks]

Continued...

(b) A counter circuit made of JK flip-flops as shown in Figure Q3B is given.

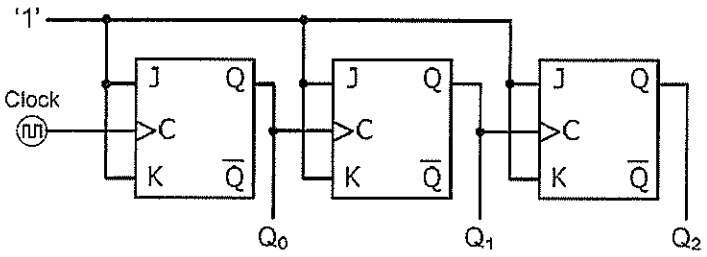

Figure Q3B

(i) Based on the circuit configuration as in Figure Q3B, justify the counter is a synchronous or asynchronous counter. Support your answer with brief explanation and state the disadvantage of this kind of counter.

[3 marks]

(ii) Write down the counting sequence in binary form together with its MOD number.

[3 marks]

(iii) Draw an alternative implementation of the counter using the same flip-flops with the same counting sequence without the disadvantage as mentioned in part (i).

[3 marks]

Continued...

Question 4

(a) A 2-bit comparator is given with the input of X and Y. These two inputs are compared and the output, F is 1 whenever X larger than Y. Find the truth table of the comparator and draw the comparator circuit with minimize resources.

[6 marks]

(b) Implement the following pair of expressions by using the given logic gates with active low output 3-to-8 line decoder.

$f_1(x_2, x_1, x_0) = \sum m(1,2,3)$ by using NOR gate only
$f_2(x_2, x_1, x_0) = \sum m(3,6,7)$ by using OR gate only

[5 marks]

(c) An 8-bit signed arithmetic operation is carried out in a binary adder. Based on the 8-bit binary adder, define what is arithmetic overflow with the supporting of example. State two methods of detecting the arithmetic overflow.

[7 marks]

(d) By using 4-to-1 multiplexer, realize the expression $F(A,B,C) = \sum m(2,4,6,7)$ and pick only C as the data input.

[7 marks]

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